AMENDMENTS TO THE CLAIMS

1. (currently amended) A method of forming an interconnect line in an integrated circuit, the method comprising:

depositing a capping layer over a metallization level;

depositing a support layer over the capping layer, the support layer being configured to provide structural support to a subsequently formed first interconnect line after an air core is formed over the metallization level;

depositing a sacrificial layer over the support layer ~~overlying a metallization level~~;

forming an opening ~~in~~ through the sacrificial layer, the support layer, and the capping layer;

depositing a metal in the opening, ~~the metal being coupled to an interconnect line in the metallization level~~ the metal serving as the first interconnect line and a via connection to a second interconnect line in the metallization level; and

etching the sacrificial layer using a chemistry that includes a noble gas fluoride to create ~~an~~ the air core ~~overlying~~ over the metallization level.

2. (currently amended) The method of claim 1 further comprising the act of planarizing the metal prior to ~~exposing~~ etching the sacrificial layer.

3. (currently amended) The method of claim 1 further comprising the act of depositing a topside layer over the metal after etching of the sacrificial layer ~~overlying the air core~~.

4. (canceled)

5. (canceled)

6. (original) The method of claim 1 wherein the opening includes a via.

7. (original) The method of claim 1 wherein the metal includes copper.

8. (original) The method of claim 1 wherein the noble gas fluoride includes xenon difluoride.

9. (original) The method of claim 1 wherein the sacrificial layer includes polycrystalline silicon.

10. (original) The method of claim 4 wherein the capping layer includes silicon nitride.

11. (original) The method of claim 1 wherein the metallization level includes a damascene structure.

12-20 (canceled)

21. (new) A method of forming a metal structure in a dual-damascene process for fabricating an integrated circuit, the method comprising:

depositing a support layer over a first metallization level of the integrated circuit, the support layer being configured to provide structural support to a subsequently formed interconnect line in a second metallization level after an air core is formed over the first metallization level;

depositing a sacrificial layer over the support layer;

forming a via and an interconnect line pattern in the sacrificial layer;

depositing a metal in the via and in the interconnect line pattern, the metal serving as a metal layer of the second metallization level and forming a via connection to the first metallization level;

planarizing the metal; and

etching the sacrificial layer using a noble gas fluoride etchant to form the air core between the first metallization level and the second metallization level.

22. (new) The method of claim 21 wherein the sacrificial layer comprises polycrystalline silicon.

23. (new) The method of claim 21 wherein the metal comprises copper.

24. (new) The method of claim 21 wherein the noble gas fluoride comprises xenon difluoride.

25. (new) The method of claim 21 further comprising:

prior to etching the sacrificial layer, depositing a capping layer over the metal.

26. (new) The method of claim 21 further comprising:

depositing a non-conductive layer over the sacrificial layer before depositing the metal in the via and in the interconnect line pattern;

wherein the via extends through the non-conductive layer, the sacrificial layer, and the support layer.

27 (new) The method of claim 26 wherein the support layer is over a capping layer and wherein the via extends through the non-conductive layer, the sacrificial layer, the support layer, and the capping layer.